Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17339	texas adj instruments.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:12
L2	97	(texas adj instruments).as. and ((second other subsequent additional) and (register cache memory) and (information data) and instruction and current and (consumption usage) and (tariff tax fee rate) and system and (computation calculation calculating calculate compute calculated computing computed) and (electricity energy) and (consumed used))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:15
L3	4	(texas adj instruments).as. and (first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) and (input interface entry) and (sensor transducer detector probe) and (memory cache register) and (second subsequent additional other) and ((bus adj system) fieldbus profibus modbus cebus rambus) and instruction and (program algorithm software firmware)) and (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:17
L4	0	(texas adj instruments).as. and ((second other subsequent additional) same (register cache memory) same (information data) same instruction same current same (consumption usage) same (tariff tax fee rate) same system same (computation calculation calculating calculate compute calculated computing computed) same (electricity energy) and (consumed used))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:16
L5	0	(texas adj instruments).as. and (first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) same (input interface entry) same (sensor transducer detector probe) same (memory cache register) same (second subsequent additional other) same ((bus adj system) fieldbus profibus modbus cebus rambus) same instruction same (program algorithm software firmware)) same (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:18

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	65646	g06f019/00.ipc.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/02 08:20
L2	219	g06f019/00.ipc. and ((second other subsequent additional) and (register cache memory) and (information data) and instruction and current and (consumption usage) and (tariff tax fee rate) and system and (computation calculation calculating calculate compute calculated computing computed) and (electricity energy) and (consumed used))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:22
L3	9	g06f019/00.ipc. and (first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) and (input interface entry) and (sensor transducer detector probe) and (memory cache register) and (second subsequent additional other) and ((bus adj system) fieldbus profibus modbus cebus rambus) and instruction and (program algorithm software firmware)) and (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:21
L4	0	g06f019/00.ipc. and ((second other subsequent additional) same (register cache memory) same (information data) same instruction same current same (consumption usage) same (tariff tax fee rate) same system same (computation calculation calculating calculate compute calculated computing computed) same (electricity energy) and (consumed used))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:21
L5	0	g06f019/00.ipc. and (first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) same (input interface entry) same (sensor transducer detector probe) same (memory cache register) same (second subsequent additional other) same ((bus adj system) fieldbus profibus modbus cebus rambus) same instruction same (program algorithm software firmware)) same (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 08:21

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	73/1.24.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:32
L2	605	137/386.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:32
L3	178	222/21.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L4	117	250/356.1.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L5	456	324/204.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L6	612	700/282.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L7	266	702/33.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L8	473	702/45.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L9	211	702/47.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L10	330	702/50.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:33
L11	28	702/53.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:34
L12	327	702/127.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:34
L13	759	702/188.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:34
L14	626	702/189.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/02 08:34
L15	59	(l1 l2 l3 l4 l5 l6 l7 l8 l9 l10 l11 l12 l13 l14) and ((second other subsequent additional) and (register cache memory) and (information data) and instruction and current and (consumption usage) and (tariff tax fee rate) and system and (computation calculation calculating calculate compute calculated computing computed) and (electricity energy) and (consumed used))	US-PGPUB; USPAT; USOCR	OR	ON	2005/08/02 08:40

L16	5	(I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14) and (first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) and (input interface entry) and (sensor transducer detector probe) and (memory cache register) and (second subsequent additional other) and ((bus adj system) fieldbus profibus modbus cebus rambus) and instruction and (program algorithm software firmware)) and (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware))	US-PGPUB; USPAT; USOCR	OR	ON	2005/08/02 08:40
L17	4	(I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14) and (first and (micro$controller micro$computer micro$processor processor controller computer (programmable adj logic adj (unit controller system device))) and (input interface entry) and (sensor transducer detector probe) and (memory cache register) and (second subsequent additional other) and ((bus adj system) fieldbus profibus modbus cebus rambus) and instruction and (program algorithm software firmware)) and (first with (second subsequent additional other) with (memory cache register) with (data information) with (program algorithm software firmware)). clm.	US-PGPUB; USPAT; USOCR	OR	ON	2005/08/02 08:41
L18	1	(I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12 I13 I14) and ((second other subsequent additional) and (register cache memory) and (information data) and instruction and current and (consumption usage) and (tariff tax fee rate) and system and (computation calculation calculating calculate compute calculated computing computed) and (electricity energy) and (consumed used)). clm.	US-PGPUB; USPAT; USOCR	OR	ON	2005/08/02 08:40